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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,390	09/15/2004	Cheng-Hsiung Chen	NAUP0527USA	5389

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EXAMINER
HO, TU TU V

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 01/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/711,390	CHEN ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2004 and 02 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) *1-6* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *3,10 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 10711390 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention I, claims 1-15, and cancellation of claims 16-20, in the reply filed on 01/02/2006 is acknowledged.

Drawings

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "ion implantation well" of **claims 4 and 13** and the "dielectric layer" of **claims 6 and 15** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the

renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

4. **Claims 3 and 12** are objected to because of the following informalities: Each of said claims recites "inter layer" (three occurrences) which should be either "interlayer" or "inter-layer". Appropriate correction is required.

Claim Interpretations

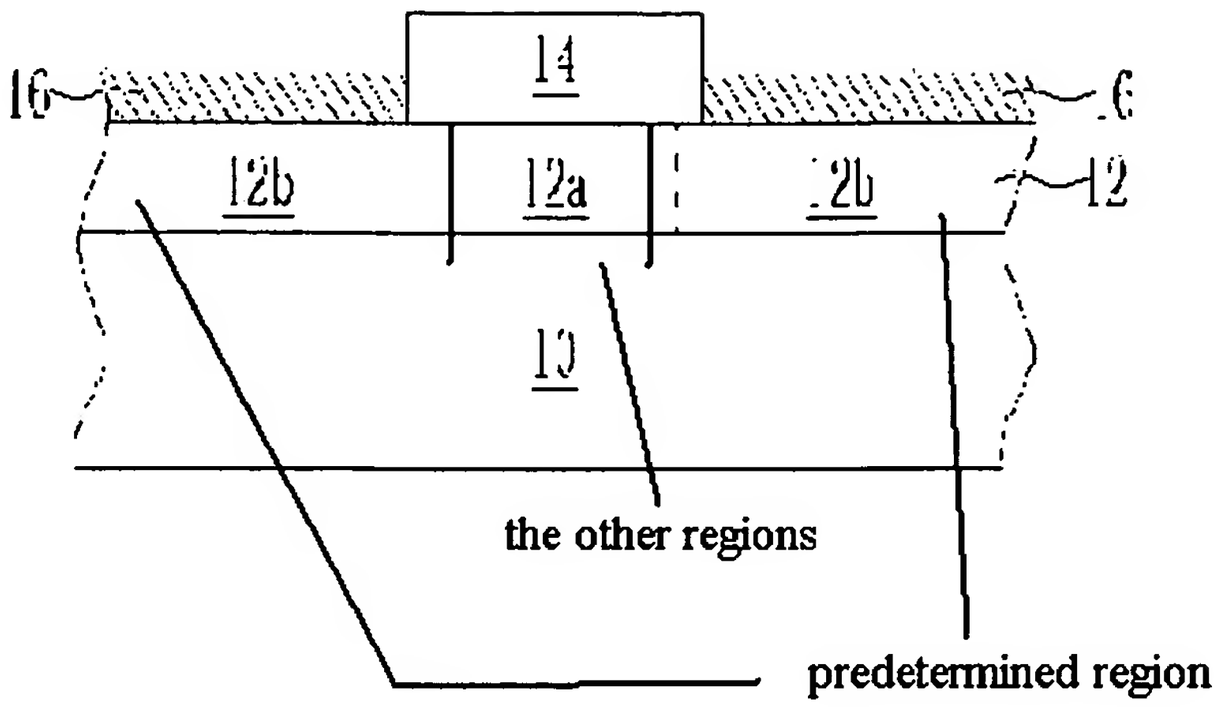
5. **Claim 7** recites:

a resistor structure comprising:

a substrate; and

a semiconductor layer positioned on the substrate, the semiconductor layer comprising at least a high resistance region and a low resistance region;

wherein the semiconductor layer comprises a predetermined region overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region, and the semiconductor layer has a higher doping concentration within the predetermined region than in the other regions.



As such, the semiconductor layer is generally indicated at 12b/12a/12b (Fig. 1 or Fig. 4 of the present application), the high resistance region is generally indicated at 12a, the low resistance region is generally indicated at 12b, "the other regions" is generally indicated at "the other regions" of Fig. 4 of the present application, reproduced above or in a previous page, and the "predetermined region" is generally indicated at "predetermined region"; and as such, it is clear that the claim does not require that the "higher doping concentration" is present in all of the predetermined region, because the predetermined region overlaps portion of the high resistance region (12a, which has a lower doping concentration, as is known in the art and as disclosed by Applicant) adjacent to the junction between the low resistance region (12b) and the high resistance region (12a).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. **Claims 7 and 11-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Sato et al. U.S. Patent 5,607,866 (the '866 reference).

Referring to **claim 7**, the '866 reference discloses a resistor structure comprising:

a substrate (generally indicated at 1A,1B, Fig. 17); and

a semiconductor layer (generally indicated at 22R/14R/22R) positioned on the substrate, the semiconductor layer comprising at least a high resistance region (14R, p doped, as is known in the art and as disclosed by Applicant) and a low resistance region (22R, p+ doped, as is known in the art and as disclosed by Applicant);

wherein the semiconductor layer comprises a predetermined region (generally defined by a region of the semiconductor layer not including a portion of the high resistance region 14R) overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region, and the semiconductor layer has a higher doping concentration (p+) within the predetermined region than in the other regions (which has a p doping) (and see note in the claim interpretations section above).

Referring to **claim 11**, the reference further discloses that the predetermined region (generally defined by a region of the semiconductor layer not including a portion of the high

resistance region 14R) is located at either end of the semiconductor layer (generally indicated at 22R/14R/22R).

Referring to **claim 12**, the reference further discloses an interlayer dielectric (25) positioned on the substrate, the interlayer dielectric comprising at least a contact hole (25bR) connecting to the portions of the semiconductor layer within the low resistance region (22R); and at least a conductive layer (26R) positioned on portions of the surface of the inter layer dielectric and within the contact hole.

Referring to **claim 13**, the reference further discloses an ion implantation well (n- well 2R) positioned underneath the semiconductor layer.

7. Claims 7, 11, and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al. U.S. Patent Application Publication 20050074929 (the '929 reference).

The '929 reference discloses in the figures, particularly Fig. 1, and respective portions of the specification a resistor structure as claimed.

Referring to **claim 7**, the '929 reference discloses a resistor structure (generally indicated at 116 or 117, Fig. 1) comprising:

a substrate (generally indicated at 101, Fig. 1); and

a semiconductor layer (generally indicated at 108/110/108, 109/111/109) positioned on the substrate, the semiconductor layer comprising at least a high resistance region (110, paragraph [0029]) and a low resistance region (108, "high concentration impurity" region, as is known in the art and as disclosed by Applicant);

wherein the semiconductor layer comprises a predetermined region (generally defined by a region of the semiconductor layer not including a portion of the high resistance region 110) overlapping the low resistance region, the junction between the low resistance region and the high resistance region, and the portions of the high resistance region adjacent to the junction between the low resistance region and the high resistance region, and the semiconductor layer has a higher doping concentration ("high concentration impurity" region 108) within the predetermined region than in the other regions (which comprises a portion or portions of the high resistance region 110) (also see note in the claim interpretations section above).

Referring to **claim 11**, the reference further discloses that the predetermined region (generally defined by a region of the semiconductor layer not including a portion of the high resistance region 110) is located at either end of the semiconductor layer (generally indicated at 108/110/108, 109/111/109).

Referring to **claim 13**, the reference further discloses an ion implantation well (n- well 102, paragraph [0027]) positioned underneath the semiconductor layer (generally indicated at 108/110/108, 109/111/109).

Referring to **claim 14**, the reference further discloses that the semiconductor layer comprises a polysilicon layer (paragraph [0028]).

Referring to **claim 15**, the reference further discloses a dielectric layer (106, paragraph [0028]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 8-9** are rejected under 35 U.S.C. §103(a) as being unpatentable over Sato et al. U.S. Patent 5,607,866 (the '866 reference) in view of Kamino et al. U.S. Patent Application Publication 20020140097 (the '097 reference).

Referring to **claims 8-9**, the '866 reference discloses a resistor structure substantially as claimed and as detailed above for claim 7, including the semiconductor layer (generally indicated at 22R/14R/22R) positioned on the substrate (1A/1B), the semiconductor layer comprising at least a high resistance region (14R) and a low resistance region (22R). The reference further discloses a salicide layer (silicide layer 24R1, col. 15, first full paragraph) positioned on the portions of the semiconductor layer within the low resistance region (22R) (in re claim 9).

However, the reference does not disclose a salicide block positioned on the portions of the semiconductor layer within the high resistance layer (14R) (in re claim 8).

The '097 reference, in also disclosing a resistor structure 2 having silicide contact layers (3) at either end of the resistor structure (Figs. 6 and 2), which contact regions are silicide layers (paragraphs [0008], [0009], [0036]) and which are functionally the same as silicide layers 24R1, 24R2 of the '866 reference, and which are functionally the same as salicide layers of the claims, discloses that in forming such silicide or salicide layers, residues of the metal that forms the silicide layers remain and diffuse into the substrate, which results in reduced yield (paragraphs [0009]-[0011]), and teaches that forming at least a dummy silicide layer 12, or silicide block (as "block" has not been

clearly defined, "block" is broadly interpreted as layer) in between the silicide layers 3 and on the non-silicide portion of the resistor (which non-silicide portion is functionally the same as the high resistance region 14R of the '866 reference or as the high resistance region of claim 8 or as the portions of the surface of the semiconductor layer in "a salicide block positioned on the portions of the surface of the semiconductor layer" as recited in claim 1) helps efficiently capture the metal residues (paragraph [0037]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '866 reference's resistor device such that it includes a silicide block as claimed. One would have been motivated to make such a change in view of the teachings in Kamino the '097 reference that such an addition would help efficiently capture the metal residues in forming the contact silicide layers, which ultimately result in better yield.

Allowable Subject Matter

9. Claims 1-6, insofar as in compliance with the drawing objections and the claim objections noted above, are allowable over the prior art of record.

Claim 10 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a resistor structure having all exclusive limitations as recited in claim 1 and claim 10, comprising the salicide block, the salicide layer, the predetermined region, characterized in that

the predetermined region overlaps the salicide layer, the junction between the salicide layer and the salicide block, and the portions of the salicide block adjacent to the junction between the salicide layer and the salicide block, and that the semiconductor layer has a higher doping concentration within the predetermined region than in the other regions.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tu-Tu Ho
January 06, 2006